	L #	Hits	Search Text	DBs
1	L1	2580	(temporar$3 second$3) adj1 (cache ((instruction prefetch fetch) adj1 (buffer queue)))	USPAT; US-PGPUB
2	L2	3450	cache near10 (line block) near10 instruction	USPAT; US-PGPUB
3	L4	120	1 near99 2	USPAT; US-PGPUB
4	L5	532	(temporar$3 second$3) adj1 (cache ((instruction prefetch fetch) adj1 (buffer queue)))	EPO; JPO; DERWENT; IBM_TDB
5	L6	558	cache near10 (line block) near10 instruction	EPO; JPO; DERWENT; IBM_TDB
6	L7	22	5 and 6	EPO; JPO; DERWENT; IBM_TDB
7	L9	44	2 and 8	USPAT; US-PGPUB
8	L11	0	6 and 10	EPO; JPO; DERWENT; IBM_TDB
9	L10	29	(temporar$3 second$3) adj1 ((instruction prefetch fetch) adj1 (buffer queue))	EPO; JPO; DERWENT; IBM_TDB
10	L8	76	(temporar$3 second$3) adj1 ((instruction prefetch fetch) adj1 (buffer queue))	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	JP 11024942 A	☐	MICROCOMPUTER	
2	JP 10078868 A	☒	DATA PROCESSOR	
3	JP 06230963 A	☒	MEMORY ACCESS CONTROLLER	
4	JP 06187149 A	☒	INSTRUCTION FETCH CONTROL SYSTEM IN INSTRUCTION PROCESSOR	
5	JP 03166626 A	☒	INFORMATION PROCESSOR	
6	JP 02208728 A	☒	VIRTUAL INSTRUCTION CACHE RE-REPLENISHMENT ALGORITHM	
7	JP 63318634 A	☒	INSTRUCTION PREFETCHING SYSTEM	
8	JP 60181931 A	☒	INSTRUCTION PREFETCH CONTROL DEVICE	
9	JP 54122040 A	☒	ELECTRONIC COMPUTER	
10	JP 52004741 A	☒	MEMORY CONTROL SYSTEM	
11	WO 9637831 A1	☒	TWO TIER PREFETCH BUFFER STRUCTURE AND METHOD WITH BYPASS	
12	NA891 0307	☒	Dual Use of Pins to Output Internal Machine Status Information	
13	NN880 2286	☒	Single Instruction Mode for Pipelined Processor	
14	NN810 81401	☒	Shared Instruction Buffer for Multiple Instruction Streams. August 1981.	
15	NN670 41551	☒	Selective Gating of Exception Tags. April 1967.	
16	NN640 672	☒	Instruction Unit. June 1964.	
17	US 6301651 B	☒	Instruction combining apparatus for stack machine, combines operands corresponding to source and destination respectively to form respective addresses	
18	US 6122727 A	☒	Instruction scheduling mechanism in processor, evaluates intermediate scheduling request signal and dependency vector during primary phase of clock to generate request signal based on secondary instruction	
19	JP 11024942 A	☒	Microcomputer with interruption processing function - has instruction controller which switches over either first or second instruction queues that can be operated during main routine process or subroutine process of predetermined interruption, respectively.	
20	EP 1010063 B	☒	Microprocessor instruction alignment unit - Has instruction queue with position storages for identifiers	
21	US 5809272 A	☒	Variable length instruction pipelined decoder - has primary buffer dispatching instruction bytes to primary decoder, secondary decoder and secondary buffer, for determining length of subsequent instructions	
22	US 5802340 A	☒	Speculative inspection execution method for parallel processing computer system - involves speculatively completing first store instruction before second instruction when set of statuses of first store instruction and second instruction do not conflict mutually	

	Document ID	U	Title	Current OR
23	JP 10078868 A	☒	Data processor for instructions with different lengths - has instruction queues that store same instructions corresponding to bits of instruction immediate data generator, and which are doubled when queue circuits are orderly arranged in bit positions	
24	JP 09223014 A	☒	Data processor - has second decoder which decodes instruction stored from either second register or instruction queue buffer	
25	US 5608885 A	☒	Method of handling instructions from branch prior to instruction decoding in computer system. - involves alternately selecting multiplexer instructions of target instruction stream from first and second instruction buffers for input to rotator	
26	US 5619663 A	☒	Computer system e.g. single chip microcontroller with instruction prefetch scheme - has second instruction prefetch buffer in system, pref., in bus interface unit which serves as memory interface unit	
27	EP 644482 A	☒	Computer system for dispatching instructions to multiple execution units - defines instructions as dependent or independent for execution sequentially or in parallel depending upon definition and relationship to other instructions	
28	US 5226130 A	☒	Branch prediction cache with maintained consistency - organises store into instruction stream detection resulting in invalidation of corresponding cache entry data and main memory access	
29	EP 380854 A	☐	Instruction buffer system for pipelined digital computer - includes two prefetch buffers for storing a preselected number of subsequent bytes and consumes instructions in shifter	

	Document ID	U	Title	Current OR
1	US 20030225998 A1	☐	Configurable data processor with multi-length instruction set architecture	712/210
2	US 20030212879 A1	☒	Method and apparatus for object code compression and decompression for computer systems	712/208
3	US 20030005262 A1	☒	Mechanism for providing high instruction fetch bandwidth in a multi-threaded processor	712/207
4	US 20020156992 A1	☒	Information processing device and computer system	712/24
5	US 20020099964 A1	☒	Reducing power consumption by estimating engine load and reducing engine clock speed	713/320
6	US 20020087835 A1	☒	Method and apparatus for improving dispersal performance in a processor through the use of no-op ports	712/215
7	US 20010037444 A1	☒	INSTRUCTION BUFFERING MECHANISM	712/207
8	US 20010027515 A1	☒	Apparatus and method of controlling instruction fetch	712/207
9	US 6691305 B1	☒	Object code compression using different schemes for different instruction types	717/136
10	US 6578137 B2	☒	Branch and return on blocked load or store	712/228
11	US 6564309 B1	☒	DSP architecture optimized for memory accesses	711/168
12	US 6553482 B1	☒	Universal dependency vector/queue entry	712/216
13	US 6523110 B1	☒	Decoupled fetch-execute engine with static branch prediction support	712/239
14	US 6460130 B1	☒	Detecting full conditions in a queue	712/32
15	US 6386456 B1	☒	Memory card identification system	235/487
16	US 6367006 B1	☒	Predecode buffer including buffer pointer indicating another buffer for predecoding	712/244
17	US 6367002 B1	☒	Apparatus and method for fetching instructions for a program-controlled unit	712/206
18	US 6363475 B1	☒	Apparatus and method for program level parallelism in a VLIW processor	712/206
19	US 6349383 B1	☒	System for combining adjacent push/pop stack program instructions into single double push/pop stack microinstuction for execution	712/226
20	US 6308259 B1	☒	Instruction queue evaluating dependency vector in portions during different clock phases	712/214

	Document ID	U	Title	Current OR
21	US 6282630 B1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
22	US 6275921 B1	☒	Data processing device to compress and decompress VLIW instructions by selectively storing non-branch NOP instructions	712/24
23	US 6247114 B1	☒	Rapid selection of oldest eligible entry in a queue	712/216
24	US 6237074 B1	☒	Tagged prefetch and instruction decoder for variable length instruction set and method of operation	711/213
25	US 6212623 B1	☒	Universal dependency vector/queue entry	712/216
26	US 6212622 B1	☒	Mechanism for load block on store address generation	712/216
27	US 6185672 B1	☒	Method and apparatus for instruction queue compression	712/217
28	US 6170051 B1	☒	Apparatus and method for program level parallelism in a VLIW processor	712/225
29	US 6145054 A	☒	Apparatus and method for handling multiple mergeable misses in a non-blocking cache	711/119
30	US 6122727 A	☒	Symmetrical instructions queue for high clock frequency scheduling	712/214
31	US 6119220 A	☒	Method of and apparatus for supplying multiple instruction strings whose addresses are discontinued by branch instructions	712/235
32	US 6092181 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/206
33	US 6092176 A	☒	System and method for assigning tags to control instruction processing in a superscalar processor	712/23
34	US 6085311 A	☒	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/204
35	US 6058465 A	☒	Single-instruction-multiple-data processing in a multimedia signal processor	712/7
36	US 6052776 A	☒	Branch operation system where instructions are queued until preparations is ascertained to be completed and branch distance is considered as an execution condition	712/233
37	US 6021484 A	☒	Dual instruction set architecture	712/41
38	US 5968160 A	☒	Method and apparatus for processing data in multiple modes in accordance with parallelism of program by using cache memory	712/14
39	US 5951675 A	☒	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/215
40	US 5925122 A	☒	Data processing unit which pre-fetches instructions of different lengths to conduct processing	712/210
41	US 5918044 A	☒	Apparatus and method for instruction fetching using a multi-port instruction cache directory	712/235
42	US 5872946 A	☒	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/204
43	US 5864690 A	☒	Apparatus and method for register specific fill-in of register generic micro instructions within an instruction queue	712/208

	Document ID	U	Title	Current OR
44	US 5845100 A	☒	Dual instruction buffers with a bypass bus and rotator for a decoder of multiple instructions of variable length	712/204
45	US 5838984 A	☒	Single-instruction-multiple-data processing using multiple banks of vector registers	712/5
46	US 5809272 A	☒	Early instruction-length pre-decode of variable-length instructions in a superscalar processor	712/210
47	US 5784630 A	☒	Method and apparatus for processing data in multiple modes in accordance with parallelism of program by using cache memory	712/30
48	US 5771241 A	☒	Method and apparatus for embedding operand synthesizing sequences in randomly generated tests	714/733
49	US 5752263 A	☒	Apparatus and method for reducing read miss latency by predicting sequential instruction read-aheads	711/137
50	US 5692167 A	☒	Method for verifying the correct processing of pipelined instructions including branch instructions and self-modifying code in a microprocessor	712/226
51	US 5680564 A	☒	Pipelined processor with two tier prefetch buffer structure and method with bypass	712/205
52	US 5652858 A	☒	Method for prefetching pointer-type data structure and information processing apparatus therefor	711/137
53	US 5649137 A	☒	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
54	US 5638526 A	☒	Apparatus for operand data bypassing having previous operand storage register connected between arithmetic input selector and arithmetic unit	712/218
55	US 5613080 A	☒	Multiple execution unit dispatch with instruction shifting between first and second instruction buffers based upon data dependency	712/214
56	US 5608885 A	☒	Method for handling instructions from a branch prior to instruction decoding in a computer which executes variable-length instructions	712/204
57	US 5606676 A	☒	Branch prediction and resolution apparatus for a superscalar computer processor	712/239
58	US 5598546 A	☒	Dual-architecture super-scalar pipeline	712/209
59	US 5517657 A	☒	Segment register file read and write pipeline	711/169
60	US 5511175 A	☒	Method an apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/216
61	US 5511172 A	☒	Speculative execution processor	712/235
62	US 5442756 A	☒	Branch prediction and resolution apparatus for a superscalar computer processor	712/238
63	US 5335330 A	☒	Information processing apparatus with optimization programming	712/241
64	US 5267350 A	☒	Method for fetching plural instructions using single fetch request in accordance with empty state of instruction buffers and setting of flag latches	712/205
65	US 5263169 A	☒	Bus arbitration and resource management for concurrent vector signal processor architecture	712/7
66	US 5150470 A	☒	Data processing system with instruction queue having tags indicating outstanding data status	712/217

	Document ID	U	Title	Current OR
67	US 5113515 A	☒	Virtual instruction cache system using length responsive decoded instruction shifting and merging with prefetch buffer outputs to fill instruction buffer	711/125
68	US 4974155 A	☒	Variable delay branch system	712/219
69	US 4929085 A	☒	Image data rotation processing method and apparatus therefor	345/658
70	US 4918439 A	☒	Remote control device	340/825.69
71	US 4873643 A	☒	Interactive design terminal for custom imprinted articles	700/103
72	US 4313158 A	☒	Cache apparatus for enabling overlap of instruction fetch operations	711/140
73	US 4312036 A	☒	Instruction buffer apparatus of a cache unit	711/3
74	US 3771138 A	☒	APPARATUS AND METHOD FOR SERIALIZING INSTRUCTIONS FROM TWO INDEPENDENT INSTRUCTION STREAMS	712/205
75	US 3764988 A	☒	INSTRUCTION PROCESSING DEVICE USING ADVANCED CONTROL SYSTEM	712/234
76	US 3626427 A	☐	LARGE-SCALE DATA PROCESSING SYSTEM	712/244

	L #	Hits	Search Text	DBs
1	L1	3022	cache near5 (line block) near10 instruction	USPAT; US-PGPUB
2	L2	2176	(second$3 remain$3) adj (group portion part$5 set) adj5 instruction	USPAT; US-PGPUB
3	L3	14810	(instruction prefetch$3 fetch$3) near5 (buffer queue)	USPAT; US-PGPUB
4	L4	115122	(temporar$4 second$3) adj2 (memory storage cache buffer)	USPAT; US-PGPUB
5	L5	1	1 near50 (2 near20 4 near20 3)	USPAT; US-PGPUB
6	L6	27	1 near50 (4 near20 3)	USPAT; US-PGPUB
7	L7	3	1 near50 (4 near20 2) not 6	USPAT; US-PGPUB
8	L8	3450	cache near10 (line block) near10 instruction	USPAT; US-PGPUB
9	L9	4	8 near50 (4 near20 (2 3)) not (6 7)	USPAT; US-PGPUB
10	L10	2	8 near50 (thread$3 multithread$3) near50 3	USPAT; US-PGPUB
11	L12	235019	(temporar$4 second$3) near5 (memory storage cache buffer)	USPAT; US-PGPUB
12	L13	6606	(second$3 remain$3) near5 (group portion part$5 set) near5 instruction	USPAT; US-PGPUB
13	L15	24	8 near99 (3 near50 (12 13)) not (5 6 7 9 10)	USPAT; US-PGPUB
14	L16	1508	(plural plurality multiple multiplicity several two second) adj5 ((instruction program) adj2 (counter pointer))	USPAT; US-PGPUB
15	L18	37	8 near99 3 and 16	USPAT; US-PGPUB
16	L19	558	cache near10 (line block) near10 instruction	EPO; JPO; DERWENT; IBM_TDB
17	L20	88126	(temporar$4 second$3) near5 (memory storage cache buffer)	EPO; JPO; DERWENT; IBM_TDB
18	L21	953	(second$3 remain$3) near5 (group portion part$5 set) near5 instruction	EPO; JPO; DERWENT; IBM_TDB
19	L22	5443	(instruction prefetch$3 fetch$3) near5 (buffer queue)	EPO; JPO; DERWENT; IBM_TDB
20	L23	4	19 near99 (22 near50 (20 21))	EPO; JPO; DERWENT; IBM_TDB
21	L24	303	(plural plurality multiple multiplicity several two second) adj5 ((instruction program) adj2 (counter pointer))	EPO; JPO; DERWENT; IBM_TDB
22	L25	0	19 near99 22 and 24	EPO; JPO; DERWENT; IBM_TDB
23	L34	36	19 near99 (20 21)	EPO; JPO; DERWENT; IBM_TDB
24	L36	1	19 and 22 and (thread$3 multithread$3)	EPO; JPO; DERWENT; IBM_TDB
25	L37	82	(two second) adj2 (tier level) near50 3	USPAT; US-PGPUB

	L #	Hits	Search Text	DBs
26	L39	8	(two second) adj2 (tier level) near50 22	EPO; JPO; DERWENT; IBM_TDB
27	L38	24	8 and 37	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20040 01567 5 A1	☐	SMC detection and reverse translation in a translation lookaside buffer	711/207
2	US 20030 22976 3 A1	☒	Apparatus and method for renaming a data block within a cache	711/137
3	US 20030 20865 9 A1	☒	Information processing system with prefetch instructions having indicator bits specifying cache levels for prefetching	711/122
4	US 20030 19604 5 A1	☒	Processing device which prefetches instruction having indicator bits specifying a quantity of operand data for prefetching	711/137
5	US 20030 19604 4 A1	☒	Cache-line reuse-buffer	711/137
6	US 20030 19192 3 A1	☒	INSTRUCTION CACHE ASSOCIATIVE CROSSBAR SWITCH	712/23
7	US 20030 19189 7 A1	☒	Instruction cache apparatus and method using instruction read buffer	711/125
8	US 20030 12637 5 A1	☒	Coherency techniques for suspending execution of a thread until a specified memory access occurs	711/145
9	US 20030 07911 2 A1	☒	Instruction cache association crossbar switch	709/213
10	US 20030 07909 0 A1	☒	Instructions for test & set with selectively enabled cache invalidate	711/140
11	US 20030 06588 7 A1	☒	Memory access latency hiding with hint buffer	711/137
12	US 20030 00526 2 A1	☒	Mechanism for providing high instruction fetch bandwidth in a multi-threaded processor	712/207
13	US 20020 19446 1 A1	☒	Speculative branch target address cache	712/238
14	US 20020 18880 5 A1	☒	Mechanism for implementing cache line fills	711/119
15	US 20020 17430 3 A1	☒	BRANCH-PREDICTION DRIVEN INSTRUCTION PREFETCH	711/137
16	US 20020 17430 2 A1	☒	System and method for managing storage space of a cache	711/130
17	US 20020 14787 2 A1	☒	Sequentially performed compound compare-and-swap	710/200

	Document ID	U	Title	Current OR
18	US 20020 12924 4 A1	☒	Method for securing software via late stage processor instruction decryption	713/165
19	US 20020 11656 7 A1	☒	Efficient I-cache structure to support instructions crossing line boundaries	711/3
20	US 20020 11212 2 A1	☒	Verifying cumulative ordering	711/119
21	US 20020 08327 3 A1	☒	Information processing system with prefetch instructions having indicator bits specifying cache levels for prefetching	711/137
22	US 20020 08327 2 A1	☒	INFORMATION PROCESSING SYSTEM WITH PREFETCH INSTRUCTIONS HAVING INDICATOR BITS SPECIFYING CACHE LEVELS FOR PREFETCHING	711/137
23	US 20020 04286 2 A1	☒	Method and apparatus for data compression and decompression for a data processor system	711/125
24	US 20020 01991 2 A1	☒	Multi-port cache memory	711/131
25	US 66622 73 B1	☒	Least critical used replacement with critical cache	711/133
26	US 66548 56 B2	☒	System and method for managing storage space of a cache	711/133
27	US 65981 27 B2	☒	Information processing system with prefetch instructions having indicator bits specifying a quantity of operand data for prefetching	711/137
28	US 65981 26 B2	☒	Processing device which prefetches instructions having indicator bits specifying cache levels for prefetching	711/137
29	US 65947 34 B1	☒	Method and apparatus for self modifying code detection using a translation lookaside buffer	711/146
30	US 65947 28 B1	☒	Cache memory with dual-way arrays and multiplexed parallel output	711/127
31	US 65811 38 B2	☒	Branch-prediction driven instruction prefetch	711/125
32	US 65747 09 B1	☒	System, apparatus, and method providing cache data mirroring to a data storage system	711/119
33	US 65464 64 B2	☒	Method and apparatus for increasing data rates in a data network while maintaining system coherency	711/141
34	US 65464 62 B1	☒	CLFLUSH micro-architectural implementation method and system	711/135
35	US 65157 59 B1	☒	Printer having processor with instruction cache and compressed program store	358/1.15
36	US 64906 58 B1	☒	Data prefetch technique using prefetch cache, micro-TLB, and history file	711/140
37	US 64906 57 B1	☒	Cache flush apparatus and computer system having the same	711/135

	Document ID	U	Title	Current OR
38	US 6484228 B2	☒	Method and apparatus for data compression and decompression for a data processor system	711/1
39	US 6480938 B2	☒	Efficient I-cache structure to support instructions crossing line boundaries	711/125
40	US 6427192 B1	☒	Method and apparatus for caching victimized branch predictions	711/133
41	US 6421696 B1	☒	System and method for high speed execution of Fast Fourier Transforms utilizing SIMD instructions on a general purpose processor	708/404
42	US 6385697 B1	☒	System and method for cache process	711/128
43	US 6381679 B1	☒	Information processing system with prefetch instructions having indicator bits specifying cache levels for prefetching	711/137
44	US 6374333 B1	☒	Cache coherency protocol in which a load instruction hint bit is employed to indicate deallocation of a modified cache line supplied by intervention	711/145
45	US 6367006 B1	☒	Predecode buffer including buffer pointer indicating another buffer for predecoding	712/244
46	US 6360313 B1	☒	Instruction cache associative crossbar switch	712/215
47	US 6349383 B1	☒	System for combining adjacent push/pop stack program instructions into single double push/pop stack microinstuction for execution	712/226
48	US 6347361 B1	☒	Cache coherency protocols with posted operations	711/141
49	US 6343354 B1	☒	Method and apparatus for compression, decompression, and execution of program code	711/201
50	US 6343345 B1	☒	Cache blocking of specific data to secondary cache with a first and a second OR circuit	711/138
51	US 6336168 B1	☒	System and method for merging multiple outstanding load miss instructions	711/141
52	US 6266741 B1	☒	Method and apparatus to reduce system bus latency on a cache miss with address acknowledgments	711/122
53	US 6256727 B1	☒	Method and system for fetching noncontiguous instructions in a single clock cycle	712/235
54	US 6237074 B1	☒	Tagged prefetch and instruction decoder for variable length instruction set and method of operation	711/213
55	US 6230260 B1	☒	Circuit arrangement and method of speculative instruction execution utilizing instruction history caching	712/239
56	US 6226707 B1	☒	System and method for arranging, accessing and distributing data to achieve zero cycle penalty for access crossing a cache line	711/3
57	US 6216213 B1	☒	Method and apparatus for compression, decompression, and execution of program code	711/170
58	US 6209082 B1	☒	Apparatus and method for optimizing execution of push all/pop all instructions	712/225
59	US 6189083 B1	☒	Method and apparatus for accessing a cache memory utilization distingushing bit RAMs	711/213
60	US 6131145 A	☒	Information processing unit and method for controlling a hierarchical cache utilizing indicator bits to control content of prefetching operations	711/137

	Document ID	U	Title	Current OR
61	US 6128094 A	☒	Printer having processor with instruction cache and compressed program store	358/1.15
62	US 6122729 A	☒	Prefetch buffer which stores a pointer indicating an initial predecode position	712/244
63	US 6119222 A	☒	Combined branch prediction and cache prefetch in a microprocessor	712/238
64	US 6094708 A	☒	Secondary cache write-through blocking mechanism	711/138
65	US 6076146 A	☒	Cache holding register for delayed update of a cache line into an instruction cache	711/125
66	US 6047368 A	☒	Processor architecture including grouping circuit	712/215
67	US 6044440 A	☒	System and method to provide high graphics throughput by pipelining segments of a data stream through multiple caches	711/140
68	US 6016545 A	☒	Reduced size storage apparatus for storing cache-line-related data in a high frequency microprocessor	712/238
69	US 6012125 A	☒	Superscalar microprocessor including a decoded instruction cache configured to receive partially decoded instructions	711/125
70	US 6009510 A	☒	Method and apparatus for improved aligned/misaligned data load from cache	712/204
71	US 6002875 A	☒	Method for the reduction of instruction cache miss rate using optimization data from trace data profiles	717/153
72	US 5983321 A	☒	Cache holding register for receiving instruction packets and for providing the instruction packets to a predecode unit and instruction cache	711/125
73	US 5974542 A	☒	Branch prediction unit which approximates a larger number of branch predictions using a smaller number of branch predictions and an alternate target indication	712/239
74	US 5970235 A	☒	Pre-decoded instruction cache and method therefor particularly suitable for variable byte-length instructions	712/213
75	US 5966737 A	☒	Apparatus and method for serialized set prediction	711/213
76	US 5953747 A	☒	Apparatus and method for serialized set prediction	711/204
77	US 5951679 A	☒	Microprocessor circuits, systems, and methods for issuing successive iterations of a short backward branch loop in a single cycle	712/241
78	US 5941980 A	☒	Apparatus and method for parallel decoding of variable-length instructions in a superscalar pipelined data processing system	712/204
79	US 5930821 A	☒	Method and apparatus for shared cache lines in split data/code caches	711/146
80	US 5897654 A	☒	Method and system for efficiently fetching from cache during a cache fill operation	711/131
81	US 5895486 A	☒	Method and system for selectively invalidating cache lines during multiple word store operations for memory coherence	711/121
82	US 5881258 A	☒	Hardware compatibility circuit for a new processor architecture	712/209
83	US 5872946 A	☒	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/204

	Document ID	U	Title	Current OR
84	US 5860150 A	☒	Instruction pre-fetching of a cache line within a processor	711/213
85	US 5845101 A	☒	Prefetch buffer for storing instructions prior to placing the instructions in an instruction cache	712/207
86	US 5832306 A	☒	Acknowledge triggered forwarding of external block data responses in a microprocessor	710/52
87	US 5828860 A	☒	Data processing device equipped with cache memory and a storage unit for storing data between a main storage or CPU cache memory	712/207
88	US 5826053 A	☒	Speculative instruction queue and method therefor particularly suitable for variable byte-length instructions	712/210
89	US 5809529 A	☒	Prefetching of committed instructions from a memory to an instruction cache	711/137
90	US 5802323 A	☒	Transparent burst access to data having a portion residing in cache and a portion residing in memory	710/107
91	US 5796974 A	☒	Microcode patching apparatus and method	712/211
92	US 5794028 A	☒	Shared branch prediction structure	712/240
93	US 5794003 A	☒	Instruction cache associative crossbar switch system	712/215
94	US 5751981 A	☒	High performance superscalar microprocessor including a speculative instruction queue for byte-aligning CISC instructions stored in a variable byte-length format	712/204
95	US 5721864 A	☒	Prefetching instructions between caches	711/137
96	US 5701430 A	☒	Cross-cache-line compounding algorithm for scism processors	711/118
97	US 5699551 A	☒	Software invalidation in a multiple level, multiple cache system	711/207
98	US 5692167 A	☒	Method for verifying the correct processing of pipelined instructions including branch instructions and self-modifying code in a microprocessor	712/226
99	US 5689672 A	☒	Pre-decoded instruction cache and method therefor particularly suitable for variable byte-length instructions	712/213
100	US 5615167 A	☒	Method for increasing system bandwidth through an on-chip address lock register	365/230.08
101	US 5606676 A	☒	Branch prediction and resolution apparatus for a superscalar computer processor	712/239
102	US 5586276 A	☒	End bit markers for indicating the end of a variable length instruction to facilitate parallel processing of sequential instructions	712/204
103	US 5560028 A	☒	Software scheduled superscalar computer architecture	712/23
104	US 5542062 A	☒	Cache memory system employing virtual address primary instruction and data caches and physical address secondary cache	711/3
105	US 5450605 A	☒	Boundary markers for indicating the boundary of a variable length instruction to facilitate parallel processing of sequential instructions	712/23
106	US 5446850 A	☒	Cross-cache-line compounding algorithm for scism processors	712/215

	Document ID	U	Title	Current OR
107	US 5442760 A	☒	Decoded instruction cache architecture with each instruction field in multiple-instruction cache line directly connected to specific functional unit	712/215
108	US 5442756 A	☒	Branch prediction and resolution apparatus for a superscalar computer processor	712/238
109	US 5423016 A	☒	Block buffer for instruction/operand caches	711/123
110	US 5375216 A	☒	Apparatus and method for optimizing performance of a cache memory in a data processing system	711/123
111	US 5307477 A	☒	Two-level cache memory system	711/3
112	US 5305280 A	☒	Semiconductor memory device having on the same chip a plurality of memory circuits among which data transfer is performed to each other and an operating method thereof	365/230.03
113	US 5303377 A	☒	Method for compiling computer instructions for increasing instruction cache efficiency	717/155
114	US 5263142 A	☒	Input/output cache with mapped pages allocated for caching direct (virtual) memory access input/output data based on type of I/O devices	710/22
115	US 5261071 A	☒	Dual pipe cache memory with out-of-order issue capability	711/140
116	US 5257360 A	☒	Re-configurable block length cache	711/118
117	US 5170476 A	☒	Data processor having a deferred cache load	711/140
118	US 5113514 A	☒	System bus for multiprocessor computer system	711/144
119	US 5094024 A	☒	Computer system architecture implementing split instruction and operand cache line-pair-state management	711/123
120	US 4467414 A	☐	Cashe memory arrangement comprising a cashe buffer in combination with a pair of cache memories	711/119

	Document ID	U	Title	Current OR
1	JP 20031 77961 A	☐	INFORMATION PROCESSOR AND INFORMATION PROCESSING UNIT	
2	JP 20010 34533 A	☒	CACHE COHERENCY CONTROLLER, SECONDARY CACHE MEMORY, CENTRAL PROCESSOR, MULTIPROCESSING SYSTEM, PROCESSOR NODE, AND CACHE COHERENCY CONTROL METHOD	
3	JP 20000 29693 A	☒	INSTRUCTION CACHE DEVICE AND CONTROL METHOD THEREFOR	
4	JP 10083 347 A	☒	CACHE MEMORY DEVICE	
5	JP 09128 293 A	☒	INFORMATION PROCESSOR	
6	JP 07281 957 A	☒	CACHE STORAGE AND ACCESS INSTRUCTION GENERATION METHOD	
7	JP 07210 463 A	☒	CACHE MEMORY SYSTEM AND DATA PROCESSOR	
8	JP 06243 038 A	☒	METHOD FOR READING AND WRITING CACHED DATA AND DEVICE FOR CACHING DATA	
9	JP 03235 145 A	☒	CACHE MEMORY DEVICE	
10	WO 99261 40 A1	☒	METHOD AND SYSTEM TO ACHIEVE ZERO CYCLE PENALTY FOR ACCESS CROSSING A CACHE LINE	
11	EP 77212 3 A2	☒	Data processing system with instruction prefetch	
12	EP 43771 2 A2	☒	Tandem cache memory.	
13	NN941 2213	☒	Dual On-Chip Instruction Cache Organization in High Speed Processors	
14	NA940 6247	☒	Instruction Placement Method to Improve Cache Behavior	
15	JP 20010 34533 A	☒	Cache coherency control apparatus in multiprocessor, switches cache line corresponding to address in exclusion control instruction to temporary ineffective condition, when the instruction is issued from processor	
16	US 61382 13 A	☒	Cache for computer systems, has control unit which places reference indication into a first state, if first prefetch cache line is requested from cache	
17	JP 20000 29693 A	☒	Branch instruction cache apparatus, includes pair of cache which stores instruction block extracted from external memory and instruction block of branch information output from external memory	
18	US 56995 51 A	☒	Invalidating line in cache in each level of multiple level, multiple cache memory system - using software invalidate instruction contg. field identifying within which cache that line is to be avoided, to by-pass address translation mechanism, and marking line as invalid in response to target address and invalidate instruction	
19	EP 77212 3 A	☒	Instruction prefetching from memory to processor instruction cache - involves prefetching cold cache instruction when asked for cache line which does not reside in primary or secondary cache	
20	EP 76379 3 A	☒	Processing system with two caches and main memory for prefetching data - by detecting in first cache access event for Line M, searching second cache for Line M, transferring Line M to first cache, if found	

	Document ID	U	Title	Current OR
21	EP 589661 A	☒	Data accessing for data processing system - involves copying data between cache lines in same cache, where copy cache line initiated using opcode of CPU instruction set, where software running on data processor invokes copy using CPU instruction	
22	EP 437712 A	☐	Tandem cache memory - has two cache memories operating in parallel and supporting each other	

	L #	Hits	Search Text	DBs
1	L1	2580	(temporar$3 second$3) adj1 (cache ((instruction prefetch fetch) adj1 (buffer queue)))	USPAT; US-PGPUB
2	L2	3450	cache near10 (line block) near10 instruction	USPAT; US-PGPUB
3	L4	120	1 near99 2	USPAT; US-PGPUB
4	L5	532	(temporar$3 second$3) adj1 (cache ((instruction prefetch fetch) adj1 (buffer queue)))	EPO; JPO; DERWENT; IBM_TDB
5	L6	558	cache near10 (line block) near10 instruction	EPO; JPO; DERWENT; IBM_TDB
6	L7	22	5 and 6	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	US 20030196044 A1	☐	Cache-line reuse-buffer	711/137
2	US 20030191897 A1	☐	Instruction cache apparatus and method using instruction read buffer	711/125
3	US 20030084273 A1	☐	Processor and method of testing a processor for hardware faults utilizing a pipeline interlocking test instruction	712/227
4	US 20030005262 A1	☐	Mechanism for providing high instruction fetch bandwidth in a multi-threaded processor	712/207
5	US 20020099926 A1	☐	Method and system for prefetching instructions in a superscalar processor	712/207
6	US 20020087849 A1	☐	Full multiprocessor speculation mechanism in a symmetric multiprocessor (smp) System	712/235
7	US 6678820 B1	☐	Processor and method for separately predicting conditional branches dependent on lock acquisition	712/239
8	US 6658558 B1	☐	Branch prediction circuit selector with instruction context related condition type determining	712/239
9	US 6553480 B1	☐	System and method for managing the execution of instruction groups having multiple executable instructions	712/23
10	US 6499097 B2	☐	Instruction fetch unit aligner for a non-power of two size VLIW instruction	712/204
11	US 6321325 B1	☐	Dual in-line buffers for an instruction fetch unit	712/204
12	US 6314509 B1	☐	Efficient method for fetching instructions having a non-power of two size	712/204
13	US 6237074 B1	☐	Tagged prefetch and instruction decoder for variable length instruction set and method of operation	711/213
14	US 6230260 B1	☐	Circuit arrangement and method of speculative instruction execution utilizing instruction history caching	712/239
15	US 5809529 A	☐	Prefetching of committed instructions from a memory to an instruction cache	711/137
16	US 5774710 A	☐	Cache line branch prediction scheme that shares among sets of a set associative cache	712/238
17	US 5752263 A	☐	Apparatus and method for reducing read miss latency by predicting sequential instruction read-aheads	711/137
18	US 5724533 A	☐	High performance instruction data path	712/205
19	US 5701430 A	☐	Cross-cache-line compounding algorithm for scism processors	711/118
20	US 5692167 A	☐	Method for verifying the correct processing of pipelined instructions including branch instructions and self-modifying code in a microprocessor	712/226
21	US 5606676 A	☐	Branch prediction and resolution apparatus for a superscalar computer processor	712/239

	Document ID	U	Title	Current OR
22	US 5581718 A	☐	Method and apparatus for selecting instructions for simultaneous execution	712/206
23	US 5446850 A	☐	Cross-cache-line compounding algorithm for scism processors	712/215
24	US 5442756 A	☐	Branch prediction and resolution apparatus for a superscalar computer processor	712/238
25	US 5423016 A	☐	Block buffer for instruction/operand caches	711/123
26	US 5317701 A	☐	Method for refilling instruction queue by reading predetermined number of instruction words comprising one or more instructions and determining the actual number of instruction words used	712/207
27	US 5263142 A	☐	Input/output cache with mapped pages allocated for caching direct (virtual) memory access input/output data based on type of I/O devices	710/22

	Document ID	U	Title	Current OR
1	US 20030 20039 6 A1	☐	Scheme for reordering instructions via an instruction caching mechanism	711/137
2	US 66091 90 B1	☒	Microprocessor with primary and secondary issue queue	712/214
3	US 65534 73 B1	☒	Byte-wise tracking on write allocate	711/169
4	US 65131 04 B1	☒	Byte-wise write allocate with retry tracking	711/169
5	US 62726 22 B1	☒	Method of and circuit for instruction/data prefetching using non-referenced prefetch cache	712/237
6	US 62508 21 B1	☒	Method and apparatus for processing branch instructions in an instruction buffer	712/238
7	US 62471 20 B1	☒	Instruction buffer for issuing instruction sets to an instruction decoder	712/238
8	US 62405 24 B1	☒	Semiconductor integrated circuit	713/500
9	US 61924 65 B1	☒	Using multiple decoders and a reorder queue to decode instructions out of order	712/212
10	US 59702 35 A	☒	Pre-decoded instruction cache and method therefor particularly suitable for variable byte-length instructions	712/213
11	US 58389 40 A	☒	Method and apparatus for rotating active instructions in a parallel data processor	712/216
12	US 58260 73 A	☒	Self-modifying code handling system	712/226
13	US 58260 53 A	☒	Speculative instruction queue and method therefor particularly suitable for variable byte-length instructions	712/210
14	US 58130 33 A	☒	Superscalar microprocessor including a cache configured to detect dependencies between accesses to the cache and another cache	711/144
15	US 57969 74 A	☒	Microcode patching apparatus and method	712/211
16	US 57874 74 A	☒	Dependency checking structure for a pair of caches which are accessed from different pipeline stages of an instruction processing pipeline	711/138
17	US 57519 81 A	☒	High performance superscalar microprocessor including a speculative instruction queue for byte-aligning CISC instructions stored in a variable byte-length format	712/204
18	US 57489 78 A	☒	Byte queue divided into multiple subqueues for optimizing instruction selection logic	712/23
19	US 56896 72 A	☒	Pre-decoded instruction cache and method therefor particularly suitable for variable byte-length instructions	712/213
20	US 56236 15 A	☒	Circuit and method for reducing prefetch cycles on microprocessors	712/238
21	US 55862 95 A	☒	Combination prefetch buffer and instruction cache	711/137
22	US 54637 48 A	☒	Instruction buffer for aligning instruction sets using boundary detection	712/204

	Document ID	U	Title	Current OR
23	US 5353426 A	☒	Cache miss buffer adapted to satisfy read requests to portions of a cache fill in progress without waiting for the cache fill to complete	711/118
24	US 5230068 A	☐	Cache memory system for dynamically altering single cache memory line as either branch target entry or pre-fetch instruction queue based upon instruction sequence	711/137

	L #	Hits	Search Text	DBs
1	L1	3022	cache near5 (line block) near10 instruction	USPAT; US-PGPUB
2	L2	2176	(second$3 remain$3) adj (group portion part$5 set) adj5 instruction	USPAT; US-PGPUB
3	L3	14810	(instruction prefetch$3 fetch$3) near5 (buffer queue)	USPAT; US-PGPUB
4	L4	115122	(temporar$4 second$3) adj2 (memory storage cache buffer)	USPAT; US-PGPUB
5	L5	1	1 near50 (2 near20 4 near20 3)	USPAT; US-PGPUB
6	L6	27	1 near50 (4 near20 3)	USPAT; US-PGPUB
7	L7	3	1 near50 (4 near20 2) not 6	USPAT; US-PGPUB
8	L8	3450	cache near10 (line block) near10 instruction	USPAT; US-PGPUB
9	L9	4	8 near50 (4 near20 (2 3)) not (6 7)	USPAT; US-PGPUB
10	L10	2	8 near50 (thread$3 multithread$3) near50 3	USPAT; US-PGPUB
11	L11	3162	(second$3 remain$3) adj5 (group portion part$5 set) adj5 instruction	USPAT; US-PGPUB
12	L12	235019	(temporar$4 second$3) near5 (memory storage cache buffer)	USPAT; US-PGPUB
13	L13	6606	(second$3 remain$3) near5 (group portion part$5 set) near5 instruction	USPAT; US-PGPUB
14	L15	24	8 near99 (3 near50 (12 13)) not (5 6 7 9 10)	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20030 00526 2 A1	☐	Mechanism for providing high instruction fetch bandwidth in a multi-threaded processor	712/207
2	US 20020 19446 4 A1	☒	Speculative branch target address cache with selective override by seconday predictor based on branch instruction type	712/239
3	US 20020 19446 3 A1	☒	Speculative hybrid branch direction predictor	712/239
4	US 20020 19446 2 A1	☒	Apparatus and method for selecting one of multiple target addresses stored in a speculative branch target address cache per instruction cache line	712/238
5	US 20020 19446 1 A1	☒	Speculative branch target address cache	712/238
6	US 20020 19446 0 A1	☒	Apparatus, system and method for detecting and correcting erroneous speculative branch target address cache branches	712/238
7	US 20020 18883 4 A1	☒	Apparatus and method for target address replacement in speculative branch target address cache	712/238
8	US 20020 18883 3 A1	☒	Dual call/return stack branch prediction system	712/236
9	US 20020 09189 2 A1	☒	Method and apparatus for efficient cache mapping of compressed VLIW instructions	711/3
10	US 65811 31 B2	☒	Method and apparatus for efficient cache mapping of compressed VLIW instructions	711/3
11	US 64876 39 B1	☒	Data cache miss lookaside buffer and method thereof	711/137
12	US 61227 29 A	☒	Prefetch buffer which stores a pointer indicating an initial predecode position	712/244
13	US 60651 15 A	☒	Processor and method for speculatively executing instructions from multiple instruction streams indicated by a branch instruction	712/235
14	US 60556 21 A	☒	Touch history table	712/207
15	US 59833 36 A	☒	Method and apparatus for packing and unpacking wide instruction word using pointers and masks to shift word syllables to designated execution units groups	712/24
16	US 59789 07 A	☒	Delayed update register for an array	712/239
17	US 59681 60 A	☒	Method and apparatus for processing data in multiple modes in accordance with parallelism of program by using cache memory	712/14
18	US 58965 17 A	☒	High performance processor employing background memory move mechanism	712/207
19	US 58871 52 A	☒	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
20	US 58812 60 A	☒	Method and apparatus for sequencing and decoding variable length instructions with an instruction boundary marker within each instruction	712/210

	Document ID	U	Title	Current OR
21	US 5860017 A	☒	Processor and method for speculatively executing instructions from multiple instruction streams indicated by a branch instruction	712/23
22	US 5859992 A	☒	Instruction alignment using a dispatch list and a latch list	712/204
23	US 5812811 A	☒	Executing speculative parallel instructions threads with forking and inter-thread communication	712/216
24	US 5778246 A	☒	Method and apparatus for efficient propagation of attribute bits in an instruction decode pipeline	712/23
25	US 5740392 A	☒	Method and apparatus for fast decoding of 00H and OFH mapped instructions	712/210
26	US 5724565 A	☒	Method and system for processing first and second sets of instructions by first and second types of processing systems	712/245
27	US 5708788 A	☒	Method for adjusting fetch program counter in response to the number of instructions fetched and issued	712/214
28	US 5623615 A	☒	Circuit and method for reducing prefetch cycles on microprocessors	712/238
29	US 5581718 A	☒	Method and apparatus for selecting instructions for simultaneous execution	712/206
30	US 5423014 A	☒	Instruction fetch unit with early instruction fetch mechanism	711/3
31	US 5317701 A	☒	Method for refilling instruction queue by reading predetermined number of instruction words comprising one or more instructions and determining the actual number of instruction words used	712/207
32	US 5113515 A	☒	Virtual instruction cache system using length responsive decoded instruction shifting and merging with prefetch buffer outputs to fill instruction buffer	711/125
33	US 4179736 A	☒	Microprogrammed computer control unit capable of efficiently executing a large repertoire of instructions for a high performance data processing unit	712/232
34	US 4161026 A	☒	Hardware controlled transfers to microprogram control apparatus and return via microinstruction restart codes	712/232
35	US 4156906 A	☒	Buffer store including control apparatus which facilitates the concurrent processing of a plurality of commands	711/128
36	US 4156279 A	☒	Microprogrammed data processing unit including a multifunction secondary control store	712/209
37	US 4156278 A	☐	Multiple control store microprogrammable control unit including multiple function register control field	712/248

	Document ID	U	Title	Current OR
1	JP 2002351814 A	☐	EXTERNAL CACHE CONTROL SYSTEM AND ITS CONTROL METHOD	
2	JP 2001034533 A	☒	CACHE COHERENCY CONTROLLER, SECONDARY CACHE MEMORY, CENTRAL PROCESSOR, MULTIPROCESSING SYSTEM, PROCESSOR NODE, AND CACHE COHERENCY CONTROL METHOD	
3	JP 2000029693 A	☒	INSTRUCTION CACHE DEVICE AND CONTROL METHOD THEREFOR	
4	JP 10083347 A	☒	CACHE MEMORY DEVICE	
5	JP 08292913 A	☐	METHOD FOR PREFETCHING INSTRUCTION WORD USING UNREFERRED PREFETCH CACHE AND CIRCUIT FOR THE SAME	
6	JP 08212133 A	☒	DATA PROCESSOR AND CACHE MEMORY CONTROL METHOD	
7	JP 06222990 A	☒	DATA PROCESSOR	
8	JP 03235145 A	☒	CACHE MEMORY DEVICE	
9	JP 03071354 A	☒	METHOD FOR PROCESSING MEMORY ACCESS REQUEST AND DEVICE THEREFOR	
10	EP 1182563 A1	☒	Cache with DMA and dirty bits	
11	EP 838755 A2	☒	Binary program conversion apparatus and method	
12	WO 9736234 A1	☒	CACHE MULTI-BLOCK TOUCH MECHANISM FOR OBJECT ORIENTED COMPUTER SYSTEM	
13	EP 772123 A2	☒	Data processing system with instruction prefetch	
14	EP 437712 A2	☒	Tandem cache memory.	
15	NA9406247	☒	Instruction Placement Method to Improve Cache Behavior	
16	US 6665767 B	☒	Digital signal processing system e.g. desktop personal computer, includes operation unit that performs program controlled cache state operation on corresponding program designated address range of cache lines	
17	US 2003005262 A	☒	Multithreaded processor for providing high instruction fetch bandwidth, has instruction buffer and temporary instruction cache to respectively receive different blocks of cache line	
18	US 6374332 B	☒	Memory system for data processing system, has write request logic associated with cache memory to receive subsequent write request from processor only if previously received write request is staged to another write request logic	
19	JP 2001034533 A	☒	Cache coherency control apparatus in multiprocessor, switches cache line corresponding to address in exclusion control instruction to temporary ineffective condition, when the instruction is issued from processor	
20	US 6101577 A	☒	Microprocessor includes branch prediction unit which receives fetch address identifying first instruction block within instruction stream	

	Document ID	U	Title	Current OR
21	JP 20000 29693 A	☒	Branch instruction cache apparatus, includes pair of cache which stores instruction block extracted from external memory and instruction block of branch information output from external memory	
22	US 59960 49 A	☒	Cache coherency protocol with recently read state for data and instructions in multi processor computer system	
23	US 58812 58 A	☒	Instruction executing system in processing system	
24	JP 10207 707 A	☒	Parallel decoding method for super scalar pipeline processor e.g. for CISC system - involves storing markers indicating related data word of each data line of variable length instruction in cache memory for identifying beginning of instruction	
25	WO 98028 18 A	☒	Data memory unit with load and store unit and coupled data cache - executes load and store instructions and includes several storage location storing outstanding store instructions and associated store data, coupled data cache has second set of storage locations storing locked cache lines	
26	US 57014 30 A	☒	Cross cache line compounding - processes instructions from 1st instruction line and 2nd instruction line to generate tag indicating instruction in 1st instruction line that can be executed in parallel with instruction in 2nd instruction line	
27	JP 09160 826 A	☐	Instruction cache memory - detects three states of line buffer for effective address of fetch instruction, based on which hit detection signal is produced for transforming instruction to cache memory	
28	EP 77212 3 A	☒	Instruction prefetching from memory to processor instruction cache - involves prefetching cold cache instruction when asked for cache line which does not reside in primary or secondary cache	
29	EP 76379 3 A	☒	Processing system with two caches and main memory for prefetching data - by detecting in first cache access event for Line M, searching second cache for Line M, transferring Line M to first cache, if found	
30	US 56030 45 A	☒	Microprocessor system with instruction cache with reserved branch target section - checks instruction cache upon request from processor, and stores item from main memory in branch target section if item is target of branch instruction	
31	US 54230 16 A	☐	Block buffer for instruction and operand caches - uses read request within instruction processor for data element not currently stored within dedicated cache memory to create read cache miss condition and initiate transfer of eight word block containing requested data element is initiated	
32	US 51685 60 A	☒	Microprocessor system with split operand and instructions cache tag stores - has system tag store with different validity bit for same data line	
33	US 52300 68 A	☐	Integrated instruction-queue and branch-target cache memory - has up to three active instruction queues each associated with sequential instruction stream started by control transfer instruction	
34	EP 43771 2 A	☒	Tandem cache memory - has two cache memories operating in parallel and supporting each other	
35	EP 41224 7 A	☒	Cache memory system for data processing system - transfers data to line buffer in response to ephemeral miss, and limits data to line access portion	
36	EP 26762 8 A	☐	Microprocessor with a cache memory	

	L #	Hits	Search Text	DBs
1	L1	3022	cache near5 (line block) near10 instruction	USPAT; US-PGPUB
2	L2	2176	(second$3 remain$3) adj (group portion part$5 set) adj5 instruction	USPAT; US-PGPUB
3	L3	14810	(instruction prefetch$3 fetch$3) near5 (buffer queue)	USPAT; US-PGPUB
4	L4	115122	(temporar$4 second$3) adj2 (memory storage cache buffer)	USPAT; US-PGPUB
5	L5	1	1 near50 (2 near20 4 near20 3)	USPAT; US-PGPUB
6	L6	27	1 near50 (4 near20 3)	USPAT; US-PGPUB
7	L7	3	1 near50 (4 near20 2) not 6	USPAT; US-PGPUB
8	L8	3450	cache near10 (line block) near10 instruction	USPAT; US-PGPUB
9	L9	4	8 near50 (4 near20 (2 3)) not (6 7)	USPAT; US-PGPUB
10	L10	2	8 near50 (thread$3 multithread$3) near50 3	USPAT; US-PGPUB
11	L12	235019	(temporar$4 second$3) near5 (memory storage cache buffer)	USPAT; US-PGPUB
12	L13	6606	(second$3 remain$3) near5 (group portion part$5 set) near5 instruction	USPAT; US-PGPUB
13	L15	24	8 near99 (3 near50 (12 13)) not (5 6 7 9 10)	USPAT; US-PGPUB
14	L16	1508	(plural plurality multiple multiplicity several two second) adj5 ((instruction program) adj2 (counter pointer))	USPAT; US-PGPUB
15	L18	37	8 near99 3 and 16	USPAT; US-PGPUB
16	L19	558	cache near10 (line block) near10 instruction	EPO; JPO; DERWENT; IBM_TDB
17	L20	88126	(temporar$4 second$3) near5 (memory storage cache buffer)	EPO; JPO; DERWENT; IBM_TDB
18	L21	953	(second$3 remain$3) near5 (group portion part$5 set) near5 instruction	EPO; JPO; DERWENT; IBM_TDB
19	L22	5443	(instruction prefetch$3 fetch$3) near5 (buffer queue)	EPO; JPO; DERWENT; IBM_TDB
20	L23	4	19 near99 (22 near50 (20 21))	EPO; JPO; DERWENT; IBM_TDB
21	L24	303	(plural plurality multiple multiplicity several two second) adj5 ((instruction program) adj2 (counter pointer))	EPO; JPO; DERWENT; IBM_TDB
22	L25	0	19 near99 22 and 24	EPO; JPO; DERWENT; IBM_TDB
23	L34	36	19 near99 (20 21)	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	JP 2001166989 A	☐	MEMORY SYSTEM HAVING PREFETCH MECHANISM AND METHOD FOR OPERATING THE SYSTEM	
2	WO 9637831 A1	☒	TWO TIER PREFETCH BUFFER STRUCTURE AND METHOD WITH BYPASS	
3	EP 329942 A2	☒	Store queue for a tightly coupled multiple processor configuration with two-level cache buffer storage.	
4	EP 851344 A	☒	Combined branch prediction and cache prefetch for microprocessor - has fetch unit that addresses first level cache memory with instruction address to retrieve instruction codes for application to instruction execution pipeline	
5	EP 772820 B	☒	Pipelined processor architecture for use in microprocessor - has controller loading instruction bytes which cannot fit into first tier buffer into second tier buffer which is also used for loading instruction cache memory	
6	EP 329942 A	☒	Store queue for tightly coupled multiple processor configuration - has several write buffers for storing instructions and data from second level store queue prior to storage in second level of cache	
7	EP 276237 B	☒	Image understanding machine using elements with gated connections - stores each pixel of loaded image in memory of each processing element receiving unique label	
8	DE 3780615 G	☐	Computer vision architecture e.g. for aircraft navigation - transforms image to symbolic form, provides high level description of image and attributes, and relationships to other objects in image	

	Document ID	U	Title	Current OR
1	US 20030191902 A1	☐	System and method for cache external writing and write shadowing	711/144
2	US 20010037444 A1	☒	INSTRUCTION BUFFERING MECHANISM	712/207
3	US 6658578 B1	☒	Microprocessors	713/324
4	US 6237074 B1	☒	Tagged prefetch and instruction decoder for variable length instruction set and method of operation	711/213
5	US 6119222 A	☒	Combined branch prediction and cache prefetch in a microprocessor	712/238
6	US 5944817 A	☒	Method and apparatus for implementing a set-associative branch target buffer	712/240
7	US 5903751 A	☒	Method and apparatus for implementing a branch target buffer in CISC processor	712/238
8	US 5872910 A	☒	Parity-error injection system for an instruction processor	714/41
9	US 5857094 A	☒	In-circuit emulator for emulating native clustruction execution of a microprocessor	703/28
10	US 5778435 A	☒	History-based prefetch cache including a time queue	711/137
11	US 5774684 A	☒	Integrated circuit with multiple functions sharing multiple internal signal buses according to distributed bus access and control arbitration	710/305
12	US 5752273 A	☒	Apparatus and method for efficiently determining addresses for misaligned data stored in memory	711/201
13	US 5752263 A	☒	Apparatus and method for reducing read miss latency by predicting sequential instruction read-aheads	711/137
14	US 5706492 A	☒	Method and apparatus for implementing a set-associative branch target buffer	712/238
15	US 5699506 A	☒	Method and apparatus for fault testing a pipelined processor	714/37
16	US 5689679 A	☒	Memory system and method for selective multi-level caching using a cache level code	711/122
17	US 5680564 A	☒	Pipelined processor with two tier prefetch buffer structure and method with bypass	712/205
18	US 5649154 A	☒	Cache memory system having secondary cache integrated with primary cache for use with VLSI circuits	711/122
19	US 5649147 A	☒	Circuit for designating instruction pointers for use by a processor decoder	711/219
20	US 5649137 A	☒	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
21	US 5574871 A	☒	Method and apparatus for implementing a set-associative branch target buffer	712/200
22	US 5113514 A	☒	System bus for multiprocessor computer system	711/144

	Document ID	U	Title	Current OR
23	US 5023776 A	☒	Store queue for a tightly coupled multiple processor configuration with two-level cache buffer storage	711/122
24	US 4807110 A	☐	Prefetching system for a cache having a second directory for sequentially accessed blocks	711/213